

WHAT IS CLAIMED IS:

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① A semiconductor device evaluation method comprising the steps of:

(a) for a plurality of insulated gate transistors with different channel lengths, determining an effective channel length L_{eff} , a gate capacitance C_g which is a capacitance between a gate and a substrate, and a fringing capacitance C_f which is a capacitance between said gate and a portion of said substrate not covered with said gate, by electrical measurement and/or calculation;

(b) plotting said gate capacitance C_g and said effective channel length L_{eff} , which have been determined in said step (a), on a graph and extending the same by extrapolation on said graph to determine gate-capacitance-vs.-effective-channel-length characteristics; and

(c) calculating a gradient A of said gate-capacitance-vs.-effective-channel-length characteristics and determining a finished gate length L_g for each of said plurality of insulated gate transistors from the equation, $L_g = (C_g - C_f)/A$.

2. The semiconductor device evaluation method according to claim 1, wherein

said step (a) prepares a design gate length L_d instead of determining said effective channel length L_{eff} by electrical measurement and/or calculation,

said step (b) plots said gate capacitance C_g and said design gate length L_d , which have been determined in said step (a), on a graph and extends the same by extrapolation on said graph to determine gate-capacitance-vs.-design-gate-length instead of determining said gate-capacitance-vs.-effective-channel-length characteristics, and

said step (c) calculates a gradient of said gate-capacitance-vs.-design-gate-length characteristics as said gradient A , instead of calculating the gradient of said gate-capacitance-vs.-effective-channel-length characteristics.

3. The semiconductor device evaluation method according to claim 1, wherein said step (b) carries out said extrapolation of said characteristics by linear approximation.

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4. The semiconductor device evaluation method according to claim 1, further comprising the steps of:

(d) determining an intercept B of said gate-capacitance-vs.-effective-channel-length characteristics; and

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(e) for said plurality of insulated gate transistors, determining a gate overlap capacitance CGDO which is a capacitance between said gate and a source/drain region covered with said gate, from the equation, $CGDO = B / (2 \cdot W) - C_f$, by using a gate width W of said gate.

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5. The semiconductor device evaluation method according to claim 1, further comprising the step of:

(f) for said plurality of insulated gate transistors, determining an effective gate insulating film thickness Toxeff from the equation, $Toxeff = W \cdot \epsilon_{ox} / A$, by using said gradient A, a gate width W of said gate, and the permittivity ϵ_{ox} of a gate insulating film.

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6. A computer-readable recording medium for recording a program which is executed by a computer either by itself or in combination with a preinstalled program in said computer, to carry out said semiconductor device evaluation method according to claim 1.

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7. A semiconductor device evaluation apparatus comprising:

a calculation section for, for a plurality of insulated gate transistors with different channel lengths, plotting an effective channel length L_{eff} and a gate capacitance C_g which is a capacitance between a gate and a substrate, on a graph and extending the same by extrapolation on said graph to determine gate-capacitance-vs.-effective-channel-length characteristics, and calculating a gradient A of said characteristics;

a first determination section for determining a finished gate length L_g for each of said plurality of insulated gate transistors from the equation, $L_g = (C_g - C_f)/A$, by using a fringing capacitance C_f which is a capacitance between said gate and a portion of said substrate not covered with said gate, said gradient A , and said gate capacitance C_g ; and

a control section for controlling said calculation section and said first determination section.

8. The semiconductor device evaluation apparatus according to claim 7, wherein

said calculation section uses a design gate length L_d instead of said effective channel length L_{eff} ,

said calculation section plots said gate capacitance C_g and said design gate length L_d on a graph and extends the same by extrapolation on said graph to determine gate-capacitance-vs.-design-gate-length characteristics, instead of determining said gate-capacitance-vs.-effective-channel-length characteristics, and

said calculation section calculates a gradient of said gate-capacitance-vs.-design-gate-length characteristics as said gradient A , instead of calculating the gradient of

said gate-capacitance-vs.-effective-channel-length characteristics.

9. The semiconductor device evaluation apparatus according to claim 7,
wherein

10. The semiconductor device evaluation apparatus according to claim 7,
wherein

said apparatus further comprising:

wherein said second determination section is also controlled by said control section.

a third determination section for, for said plurality of insulated gate transistors, determining an effective gate insulating film thickness T_{oxeff} from the equation, $T_{oxeff} = W \cdot \epsilon_{ox} / A$, by using said gradient A, a gate width W of said gate, and the

wherein said third determination section is also controlled by said control section.

12. A semiconductor device evaluation method comprising the steps of:

5 (a) while regarding a plurality of insulated gate transistors with different gate length as a plurality of resistive elements with different line widths L_g each using a gate as a resistance, determining said line width L_g for some of said plurality of resistive elements;

10 (b) for all of said plurality of resistive elements, determining a resistance R_g of said gate and an effective channel length L_{eff} by electrical measurement and/or calculation;

15 (c) plotting said line width L_g and said effective channel length L_{eff} , which have been determined in said steps (a) and (b), on a graph and extending the same by extrapolation on said graph to determine line-width-vs.-effective-channel-width characteristics; and

(d) for all of said plurality of resistive elements, determining characteristics between said line width L_g and said resistance R_g by using said line-width-vs.-effective-channel-length characteristics.

20 13. A semiconductor device evaluation method comprising the steps of:

(g) preparing a finished gate length L_g determined by said semiconductor device evaluation method according to claim 1;

(h) for each of said plurality of insulated gate transistors, determining a resistance R_g of a gate by electrical measurement and/or calculation; and

25 (i) determining characteristics between said finished gate length L_g and said

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a control section for controlling said determination section.

17. A semiconductor device manufacturing control method comprising:

a judgment step for judging whether said finished gate length L_g of each of said plurality of insulated gate transistors, obtained by said semiconductor device evaluation method according to claim 1, meets required standard,

wherein a result of judgment in said judgment step is utilized for reappraisal of manufacturing conditions of semiconductor devices.

18. A semiconductor device manufacturing method comprising

a judgment step for judging whether said finished gate length L_g of each of said plurality of insulated gate transistors, obtained by said semiconductor device evaluation method according to claim 1, meets required standards,

wherein a result of judgment in said judgment step is utilized for rejection of nonconforming products.

19. A semiconductor device manufacturing control method comprising:

a judgment step for judging whether said resistance R_g of each of said plurality of insulated gate transistors, obtained by said semiconductor device evaluation method according to claim 12, meets required standards,

wherein a result of judgment in said judgment step is utilized for reappraisal of manufacturing conditions of semiconductor devices.

20. A semiconductor device manufacturing method comprising:

a judgment step for judging whether said resistance R_g of each of said plurality of insulated gate transistors, obtained by said semiconductor device evaluation method

according to claim 12, meets required standards,

wherein a result of judgment in said judgment step is utilized for rejection of nonconforming products.

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